METHOD AND APPARATUS FOR IMPLEMENTING SIGNED MULTIPLICATION OF OPERANDS HAVING DIFFERING BIT WIDTHS WITHOUT SIGN EXTENSION OF THE MULTIPLICAND

A multiplier (42) forms a product from two signed operands without performing a sign extension of the multiplicand (A). A modified Booth's recoding of the multiplier operand (B) is begun immediately without being delayed by a sign extension operation. While recoding and partial product generation is occurring, a determination is made in parallel whether or not a sign extension adjustment term must be created. When needed, a value equal to $(-B)(2^N)$, where N is equal to a bit width of the multiplicand (A), is formed in parallel with the recoding and partial product generation. The sign extension adjustment term is coupled to a plurality of carry save adders (49, 51, 53) that compress a plurality of partial products to a sum term and a carry term. A final add stage combines the sum term and carry term to provide a product with correct sign extension.